CHECKING LAYOUT ACCURACY IN INTEGRATED CIRCUIT DESIGNS

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This is a divisional application of application Serial No. 10/199,727, titled LINE WIDTH CHECK IN LAYOUT DATABASE, filed July 19 2002 ~~(pending)~~, now Patent Number 6,769,103 which application is assigned to the assignee of the present invention and the entire contents of which are incorporated herein by reference.

BB 4/15/05

FIELD

[0002] The present invention relates generally to integrated circuit layout, and more specifically to verification of integrated circuit layouts.

BACKGROUND

[0003] Typical micron level integrated circuit manufacture requires extensive layout of components and pathways between components. The pathways between components carry signals and power back and forth between components. Some components do not require much power or do not carry much current. Pathways between these types of components can be made very small in width of the metal that carries the signals or the power. However, other components have higher power or current requirements.

[0004] As power and current requirements go up, a standard minimum line width for carrying power or current between or to those components is insufficient. Typical minimum line widths for components that do not draw much current are on the order of 0.2 microns wide. On the other hand, lines that carry power or current to or from supplies and large components may need to be on the order of 10 to 1000 microns wide. The wider lines are required to carry the current as well as to avoid resistive drops and electro migration problems.

[0005] Various software solutions exist to perform certain checking of parameters in schematics, layouts, and the like. A typical design process begins with schematic, moves to layout, and then to design and on to fabrication. Along the way, checks are typically made of parameters and the like. For example, a line width check program